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| 10/551,763 | 02/13/2006 | Amina Hamidi | 004501-820 | 4261 |

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| EXAMINER | |
|---|---|
| NGUYEN, KHIEM D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2823 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 08/01/2008 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ADIPFDD@bipc.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/551,763 | HAMIDI ET AL. | |
| | Examiner | Art Unit | |
| | KHIEM D. NGUYEN | 2823 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *7-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14 and 15* is/are allowed.

6)☒ Claim(s) *7,8 and 13* is/are rejected.

7)☒ Claim(s) *9-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Applicants' Amendment*

1. Applicants' request for reconsideration of the finality of the rejection of the last Office action mailed on March 19th, 2008 is persuasive and, therefore, the finality of that action is withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Nidan et al. (U.S. Pub. 2002/0005072).

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

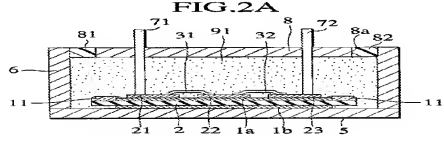
3. Claims 7, 8 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (U.S. Patent 6,201,696) in view of Nidan et al. (U.S. Pub. 2002/0005072).

In re claim 7, **Shimizu et al.** disclose a power semiconductor module, comprising: an electrically insulating substrate **2**; a first electrically conductive layer **1a** disposed on at least one portion of a top surface of said electrically insulating substrate **2**, so as to selectively expose at least one peripheral top region of said electrically insulating substrate **2** (see col. 11, line 56 to col. 12, line 8 and FIG. 2A, for example);

at least one semiconductor power chip **21/23** mounted on said first electrically conductive layer **1a** (see col. 12, lines 6-8);

a first electrically insulating material **11** disposed in a corner region formed by said first electrically conductive layer **1a** and said peripheral region of said electrically insulating substrate **2** ((see col. 12, lines 49-58 and FIG. 2A) and (col. 12, line 63 to col. 13, line 12 and FIG. 2B));

FIG.2A

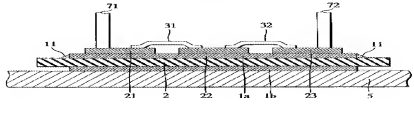



a second insulating material **91** at least partially embedding said semiconductor power chip **21/23**, said electrically insulating substrate **2**, said first electrically conductive layer **1a**, and said first electrically insulating material **11** (col. 11, lines 58-62 and FIG. 2A, for example);

wherein the first electrically insulating material **11** is a epoxy resin or polyester resin (col. 12, lines 49-58), and

the surface of the first electrically insulating material **11** disposed in the corner region formed by said first electrically conductive layer **1a** and said peripheral region of said electrically insulating substrate **2** is concave-shaped (see col. 12, line 63 to col. 13, line 12 and FIG. 2B, for example).

FIG.2B



However, **Shimizu et al.** is silent about wherein the first electrically insulating material is a polyimide.

**Nidan et al.** discloses wherein the electrically insulating material is composed of epoxy resin, polyimide resin or the like (see page 3, paragraph [0070]).

As **Nidan et al.** disclosed, one of ordinary skill in the art would have been motivated to substitute polyimide resin for epoxy resin because epoxy resin and polyimide are interchangeable. As known to one of ordinary skill in the art, thermosetting resin such as epoxy or polyester resin serve similar purpose as a thermoplastic resin such as polyimide resin.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to modify Shimizu et al. reference with an electrically insulating material composed of polyimide resin as taught by Nidan et al. since epoxy resin and polyimide resin are interchangeable in order to obtain the same result.

In re claim 8, as applied to claim 7 above, **Shimizu et al.** discloses all claimed limitations including the limitation wherein the electrically insulating substrate **2** is mounted on a bottom plate **5** (see col. 12, lines 9-13 and FIG. 2A, for example).

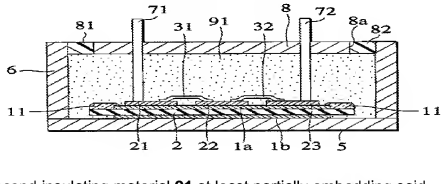
In re claim 13, **Shimizu et al.** disclose a power semiconductor module, comprising: an electrically insulating substrate **2**; a first electrically conductive layer **1a** disposed on at least one portion of a top surface of said electrically

insulating substrate **2**, so as to selectively expose at least one peripheral top region of said electrically insulating substrate **2** (see col. 11, line 56 to col. 12, line 8 and FIG. 2A, for example);

at least one semiconductor power chip **21/23** mounted on said first electrically conductive layer **1a** (see col. 12, lines 6-8);

a first electrically insulating material **11** disposed in a corner region formed by said first electrically conductive layer **1a** and said peripheral region of said electrically insulating substrate **2** ((see col. 12, lines 49-58 and FIG. 2A) and (col. 12, line 63 to col. 13, line 12 and FIG. 2B));

FIG.2A



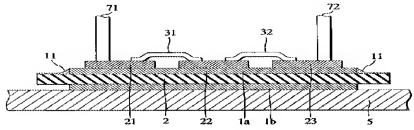

a second insulating material **91** at least partially embedding said semiconductor power chip **21/23**, said electrically insulating substrate **2**, said first electrically conductive layer **1a**, and said first electrically insulating material **11** (col. 11, lines 58-62 and FIG. 2A, for example);

wherein the first electrically insulating material **11** is a epoxy resin or polyester resin (col. 12, lines 49-58), and

the surface of the first electrically insulating material **11** disposed in the corner region formed by said first electrically conductive layer **1a** and said

peripheral region of said electrically insulating substrate **2** is concave-shaped (see col. 12, line 63 to col. 13, line 12 and FIG. 2B, for example),

FIG.2B




wherein the first electrically insulating material **11** fills gaps in a junction between the first electrically conductive layer 1a and the electrically insulating substrate **2** (see col. 12, lines 49-63 and FIG. 2A).

However, **Shimizu et al.** is silent about wherein the first electrically insulating material is a polyimide.

**Nidan et al.** discloses wherein the electrically insulating material is composed of epoxy resin, polyimide resin or the like (see page 3, paragraph [0070]).

As **Nidan et al.** disclosed, one of ordinary skill in the art would have been motivated to substitute polyimide resin for epoxy resin because epoxy resin and polyimide are interchangeable. As known to one of ordinary skill in the art, thermosetting resin such as epoxy or polyester resin serve similar purpose as a thermoplastic resin such as polyimide resin.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to modify Shimizu et al. reference with an electrically insulating material composed of polyimide resin as taught by Nidan et al. since epoxy resin and polyimide resin are interchangeable in order to obtain the same result.

***Allowable Subject Matter***

4. Claims 14-15 were previously indicated as allowable over prior art of record in Office Action mailed on March 19th, 2008.

5. Claims 9-12 were previously indicated as objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims (see Office Action mailed on March 19th, 2008).

***Response to Applicants' Amendment and Arguments***

6. Applicants' arguments with respect to claims 7, 8 and 13 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHIEM D. NGUYEN whose telephone number is (571)272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Brook Kebede/
Primary Examiner, Art Unit 2894

/Khiem D. Nguyen/
Examiner, Art Unit 2823